Amendments to the Drawings:

The attached sheets of drawings, which include figures 1-9, will replace the original sheets of drawings as filed with the application. No changes have been made.

Attachment: Replacement Sheets

Specification

Please amend the title to "Sensor Array Architecture Having Reduced Coupling Capacitance."

REMARKS/ARGUMENTS

The enclosed is responsive to the Examiner's Office Action mailed on January 26, 2006. At the time the Examiner mailed the Office Action claims 1-29, were pending and, of those, claims 23-29 were withdrawn. By way of the present response Applicants have: 1) amended claims 1, 8, 9, 11, 13-15, 20, and 22; and 2) added claims 30-38; and 3) canceled claims 6-7, and 23-29, without prejudice. As such, claims 1-5, 8-22, and 30-38 are now pending. Applicants respectfully request reconsideration of the present application and allowance of all claims now presented.

Response to § 102 Rejections

Claims 1-2, 4, 6-7, 9-17 and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Merrill (U.S. Publication No. 2002/0036700 A1) hereinafter "*Merrill*". In light of the amendment, the Examiner's rejections have become moot. Nonetheless, the following remarks regarding the Examiner's rejections and the amended claims may be helpful to expedite prosecution.

Applicant's invention relates to a photodetecting array comprising: a plurality of detecting cells **laid out** in an array on a substrate, comprising rows and columns of detecting cells; a plurality of gate lines, wherein each of the **gate lines** are coupled to a **different row** of **over two** detecting cells; a plurality of data lines, wherein each of the **data lines** are coupled to a **different column** of **over two** detecting cells; a plurality of bias voltage lines, wherein each of the bias voltage lines are coupled to a **different row of over two** detecting cells; and a plurality of additional bias voltage lines, wherein each of the **additional bias voltage lines** are coupled to **two bias voltage lines in different rows**, wherein the **gate lines** and **bias voltage lines are laid out** in a plurality of **rows** and the **data lines** and **additional bias voltage lines are laid out** in a plurality of **columns**. Applicants have recognized the advantage of reducing the **coupling capacitance** between the **bias line** and the **data line**, by forming a photodetecting array wherein the bias line and the data line are predominantly **perpendicular** to each other, **instead of parallel**. Further, Applicant has recognized the advantage of providing some additional bias voltage lines that couple adjacent bias lines, thus reducing the resistance of the bias lines, which reduces the RC time constant associated with the bias lines.

In contrast, Merrill fails to disclose or suggest the **layout** of any structure on a substrate. Merrill merely discloses schematics, which are designed to identify coupling relationships between electrical components, but is generally not intended to provide an actual **physical layout** of the structure, and thus cannot be relied upon in a rejection. Further, Merrill fails to disclose or suggest a bias line, which couples, to **over two** detecting cells in a row. In contrast, Merrill discloses a bias line that couples to **two columns** and **not to rows**. Merrill teaches away from the claimed invention by providing a bias line parallel to the data line and thus increasing the **coupling capacitance.**

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim. Nonetheless, the following remarks regarding the Examiner's rejections and the amended claims may be helpful to expedite prosecution.

Merrill fails to disclose or suggest that the **transistor** is coupled to the **gate line** and the **data line**, and wherein the **photodiode** is coupled to the **transistor** and the **bias voltage** line. In contrast Merrill discloses that the photodiode is coupled to the **ground**.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claims 1-2, 4, 6-7, 9-17 and 20-22 under 35 U.S.C. 102(b) as being anticipated by Merrill (U.S. Publication No. 2002/0036700 A1)

Response to § 103 Rejections

Claims 3, 5, 8, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Merrill* in view of Applicant's Admitted Prior Art (in Fig 1). In light of the amendment, the Examiner's rejections have become moot. Nonetheless, the following remarks regarding the Examiner's rejections and the amended claims may be helpful to expedite prosecution.

Applicant's alleged admitted prior art (AAPA) is introduced to provide the elements related to the material structure of the photodiode and that the photodiode is positioned over the transistor. However, AAPA fails remedy the deficiencies of Merrill and in fact teaches away from the invention because AAPA discloses that the bias line and the data line are parallel, and therefore would have a high coupling capacitance.

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be

interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim. Nonetheless, the following remarks regarding the Examiner's rejections and the amended claims may be helpful to expedite prosecution.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claims 3, 5, 8, 18-19 under 35 U.S.C. 103(a) as being unpatentable over *Merrill* in view of Applicant's Admitted Prior Art (in Fig 1).

Conclusion

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call James C. Scheller at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: April 26, 2006

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